Low Noise Amplifier AL33

DESCRIPTION

Sanland's AL33 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA). The LNA has low noise and high linearity achieved through the use of 0.5um GaAs Enhancement-mode pHEMT process. It is housed in a miniature 2.0 x 2.0 x 0.75mm3 8-pin Quad-Flat-Non-Lead (QFN) package. It is designed for optimum use from 400MHz up to 1.5GHz. The compact footprint and low profile coupled with low noise, high gain and high linearity make the AL33 an ideal choice as a low noise amplifier for cellular infrastructure for GSM and CDMA.

KEY FEATURES

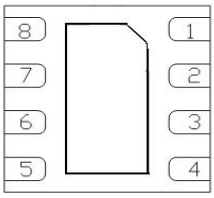
- 0.4dB noise figure at 900MHz
- 35dBm Output IP3 at 900MHz
- Optimum use from 0.4GHz up to 1.5GHz
- Small package size: 2.0 x 2.0 x 0.75mm^3
- Single 5V Supply
- ESD 250V HBM
- MSL: Level 1
- Share the same package and pin configuration with AL34 use from 1.5GHz to 2.4GHz

RoHS Compliant & Green Package

Major Applications

- LNA for cellular infrastructure and other ultra low noise application.

Pin Assignment



QFN2X2-8L

Pin Details

Pin Number	Name	Description
1	Vbias	Gate Voltage
2	RF in	RF Input
4,5,8	N/C	Good RF practice require N/C pins to be earthed
6	ENBLE	
7	RF OUT	RF output.
Exposed PAD	GND	Multiple vias should be employed to minimize inductance and thermal resistance

Electrical Characteristics for Application

(VDD =+5V; unless otherwise noted.)

Parameter	Specification			Units	Notes
	Min	Typ.	Max		
Freq	0.4		1.5	GHz	
Gain	 17.5	20.3 19.7 19.4	 21		800MHz 850MHz 900MHz
P-1dB	20 20 20	22.1 22.1 22.2			800MHz 850MHz 900MHz
OIP3	33 33 33	34.5 34.8 35			800MHz 850MHz 900MHz
Input return loss		-15 -15 -16	-10 -10 -10		800MHz 850MHz 900MHz
Output return loss		-12 -12 -12	-10 -10 -10		800MHz 850MHz 900MHz
NF		0.4 0.4 0.4	0.55 0.55 0.55		800MHz 850MHz 900MHz
Reverse Isolation		-28 -27 -27			800MHz 850MHz 900MHz
Vs		5.0	5.5	V	
Is	40	55	80	mA	

Test Conditions：VDD=5V, IDD=55mA Typ. OIP3 Tone Spacing=1MHz, Pout per ton=+5 dBm
TL=25℃, ZS=ZL=50 Ohms

Absolute Maximum Ratings

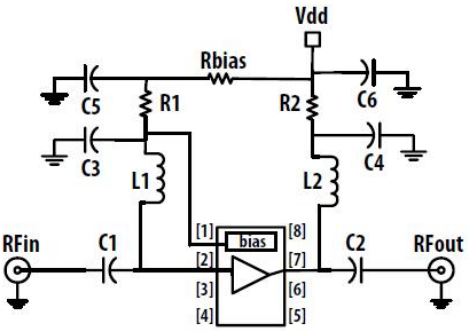
Parameter	Rating	Unit
DC Power Supply	+5.5	V
DC Supply Current at VDD	90	mA
RF Input Power	+20	dBm
Max. Operating Dissipated Power	0.5	W
Operating Ambient Temperature	-40 to +85	℃
Storage Temperature	-65 to +150	℃
Max. Junction Temp. (TJ)	+150	℃
R_{TH}	68	℃/W
Operation beyond any one of these limits may cause permanent damage.		

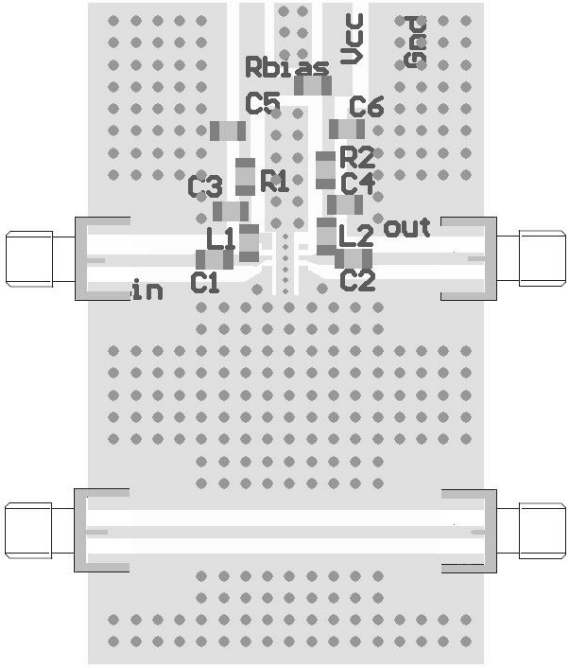
Important Note:

The information provided in this datasheet is deemed to be accurate and reliable only at present time. Sanland Technology Corp. reserves the right to make any changes to the specifications in this datasheet without prior notice.

Caution: ESD Sensitive
Appropriate precaution in handling, packaging
And testing devices must be observed.

Application Circuit





Part	Size	Value
C1, C2	0402	100pF (Murata)
L1, L2	0402	33nH (Toko)
C4	0402	33pF (Koacera)
C3, C6	0402	4.7uF (Murata)
R1	0402	0 Ohm (Kamaya)
R2	0402	10 Ohm (Koa)

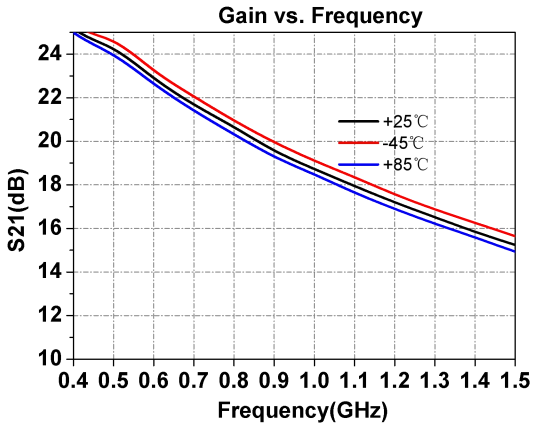
Note:

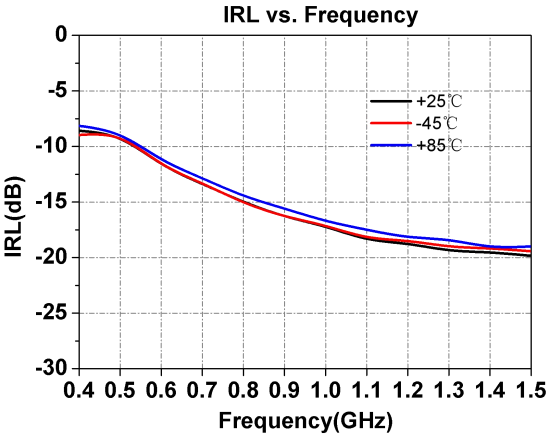
C1, C2 are DC Blocking capacitors; L1 input match for NF; L2 output match for OIP3;

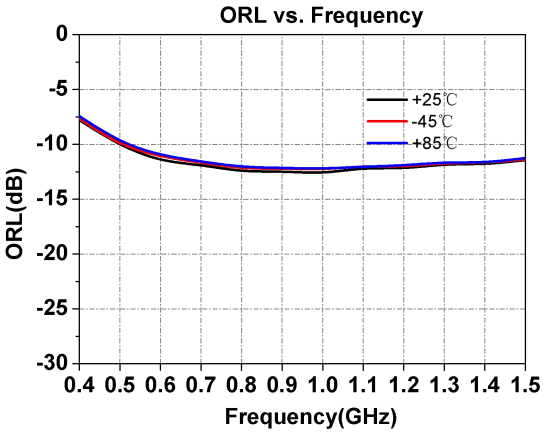
C3, C4, C6 are bypass capacitors; R2 is stabilizing resistor;

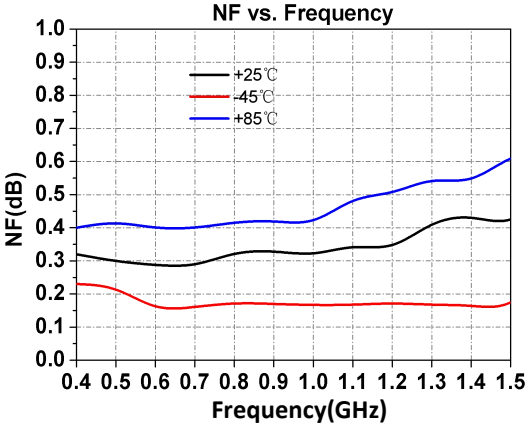
Rbias is the biasing resistor（6.8kOhm ref.）; R1, C5 are not use for this product

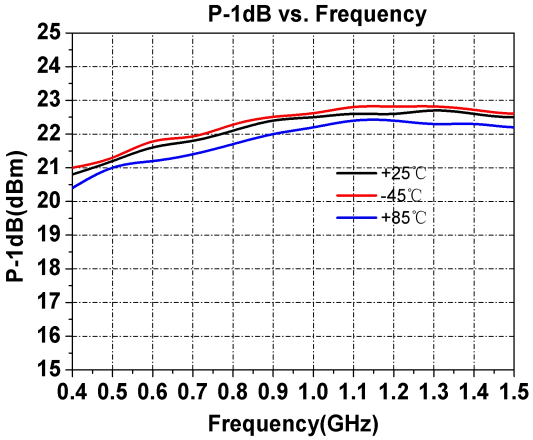
Performance Plots With Demo Board
Test conditions: VDD＝5V，Rbias＝6.8 kOhm，IDD＝55mA，Z_S=Z_L=50 Ohms。
OIP3 test conditions：OIP3 Tone Spacing=1MHz, Pout per tone=+5 dBm

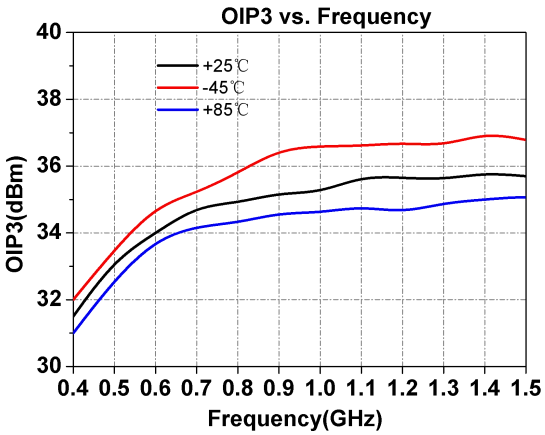


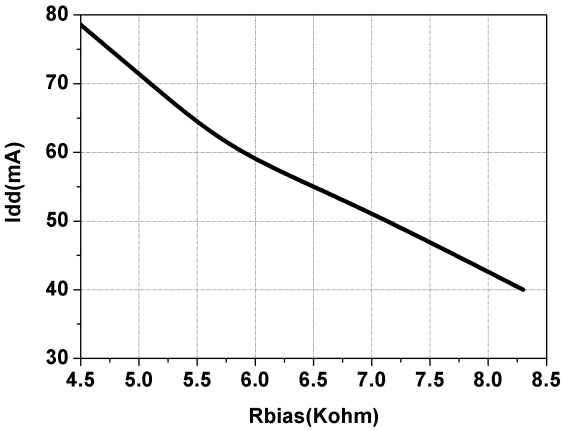


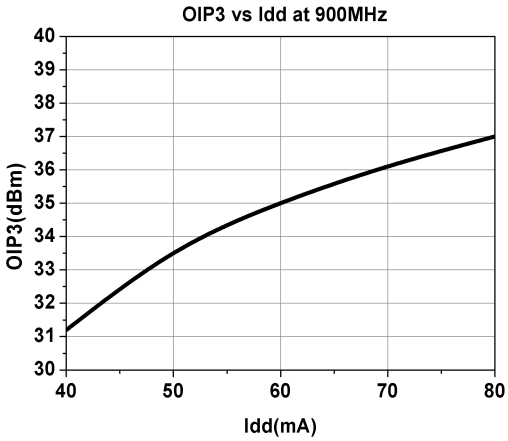


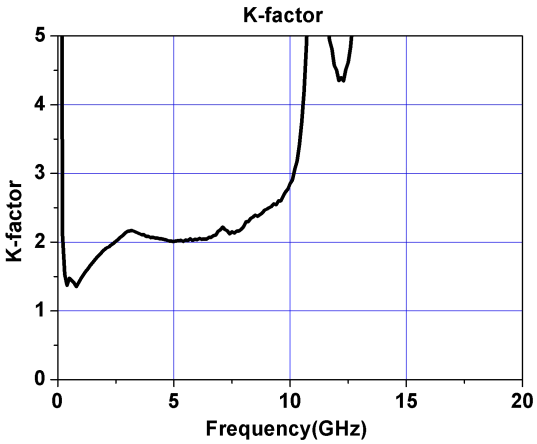






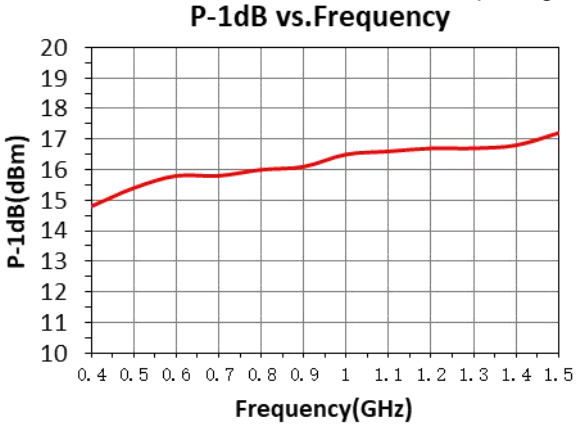


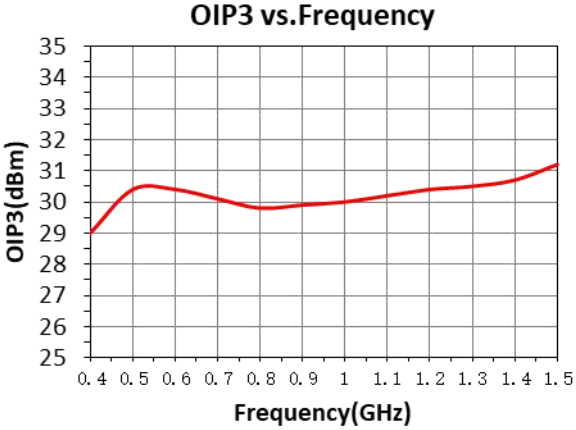




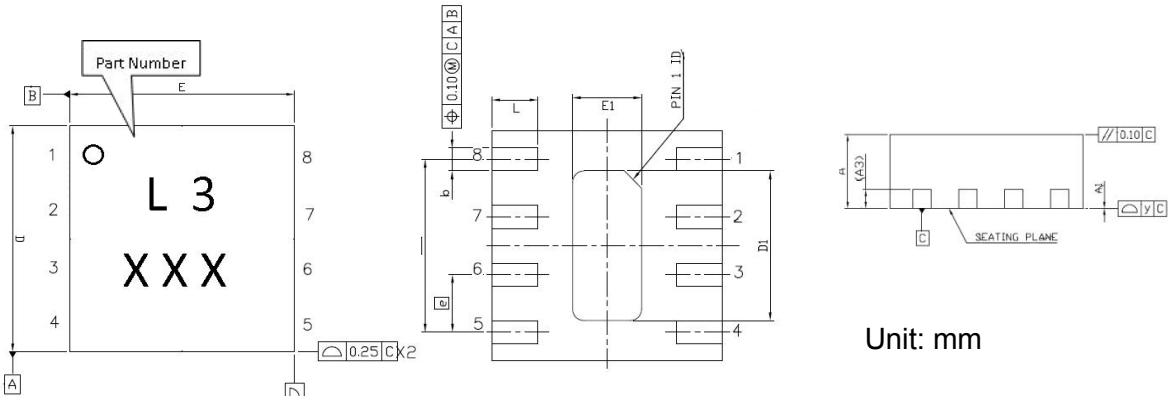
NOTE: The K-Factor tested using demo board with good RF/DC grounding. Inductance to grounding will reduce K-Factor.

Test conditions: VDD＝3.3V，Rbias＝3.6 kOhm，IDD＝50mA，Z_S=Z_L=50 Ohms。
OIP3 test conditions：OIP3 Tone Spacing=1MHz, Pout per tone=0 dBm





Package Outline

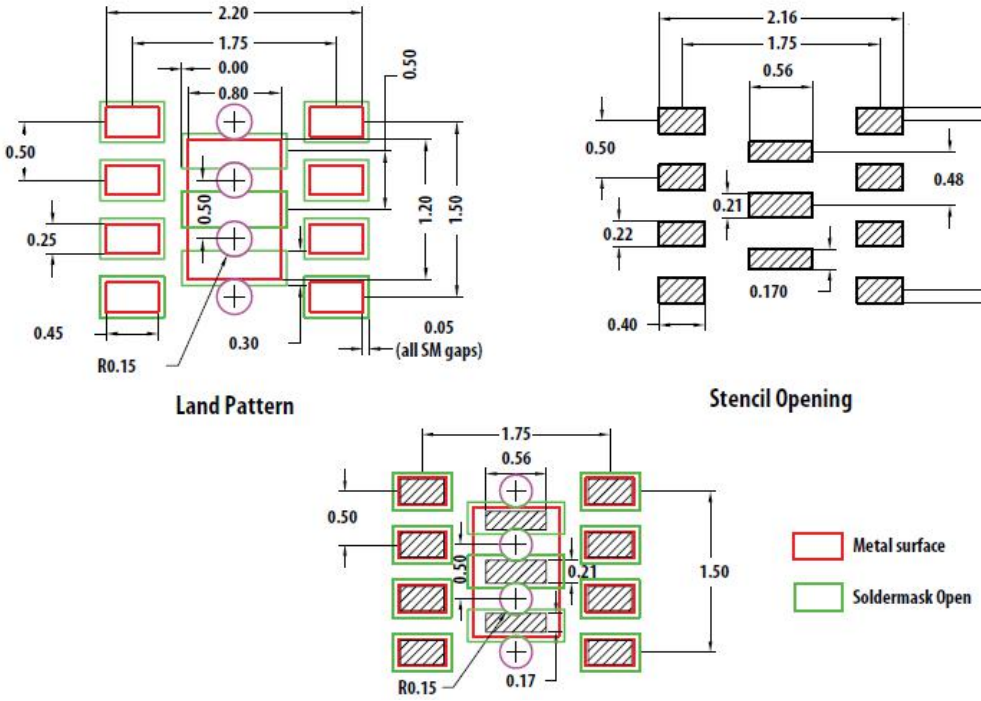


Unit: mm

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0.00	0.02	0.05	0	0.8	2
A3		0.20 REF			8 REF	
b	0.15	0.20	0.25	6	8	10
D		2.00 BSC			79 BSC	
D1	1.25	1.30	1.35	49.2	51.2	53.2
E		2.00 BSC			79 BSC	
E1	0.55	0.60	0.65	21.6	23.6	25.6
e		0.50 BSC			19.7 BSC	
e1		1.50 BSC			59 BSC	
L	0.30	0.40	0.50	11.8	15.7	19.7
y			0.08			3

Note：This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free(maximum 260℃ reflow temperature) and leaded (maximum) 245℃ reflow temperature).

Suggested PCB Layout



NOTES:

1. Dimensions are in millimeter.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under backside paddle for proper RF/DC grounding and thermal dissipation. Via holes could reduce lead inductance as close to ground as possible.
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.