

2021.12

DESCRIPTION

Sanland's AL411 is a flat gain, high linearity, ultra-low noise amplifier in a micro 2.0 x 2.0 x 0.75mm³ 8-pin DFN package. The LNA provides a gain flatness of 2dB (peak to peak) over a wide bandwidth from 2 to 4.2 GHz.

The 0.25um GaAs enhanced PHEMT technology is used to realize the low noise amplifier with low noise and high-linearity. It is packaged in a green / RoHS-compliant 2x2 mm industry standard package.

The internal active bias circuit provides stable temperature and process change performance. The LNA provides the ability to adjust the power current externally . The power supply voltage is applied to RFOUT/VDD pin through the inductance of RF choke.

Major Applications

- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

KEY FEATURES



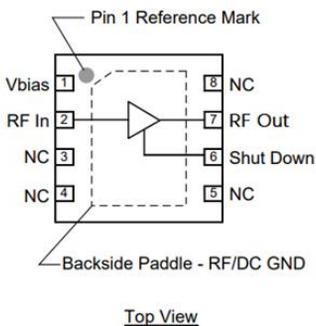
- 0.7-4.2 GHz Operational Bandwidth
- Ultra low noise figure, 0.6dB NF @ 2.6 GHz
- >20 dB gain across 0.7 to 4.2 GHz
- Flat 2 dB gain variation across 2 to 4.2 GHz.
- Bias adjustable for linearity optimization
- 33 dBm OIP3 at 55 mA IDD



ESD Class 1A

Appropriate precautions in handling , packaging and testing devices must be observed !

Pin Assignment



Pin Details

Pin Number	Name	Description
1	VBIAS	Bias voltage for input gate. External resistor sets current consumption.
2	RF in	RF input. DC blocking capacitor required.
3,4,5,8	NC	No connection. May be connected to ground with no change in performance.
6	Shut Down	
7	RFOUT/ VDD	RF output. Apply VDD through RF choke inductor. DC blocking capacitor required.

2021.12

Absolute Maximum Ratings

Parameter	Rating	Unit
DC Power Supply	+7	V
Quiescent supply current	90	mA
RF Input Power	30	dBm
Operating Temperature	-40 to +105	°C
Storage Temperature	-65 to +150	°C
Operation beyond any one of these limits may cause permanent damage.		

Thermal Data

Parameter	Specification			Units	Notes
	Min	Typ.	Max		
Thermal resistance		45		°C/W	
Channel temperature @ +85 °C reference (package heat slug)		101		°C	VDD = 5 V, IDQ = 55mA, no RF applied , dissipated power=0.275W
Test Conditions: VDD = 5 V, TA = +25 °C, PIN = -25 dBm , Characteristic Impedance [ZO] = 50 Ω, Unless Otherwise Noted.					

Important Note:

The information provided in this datasheet is deemed to be accurate and reliable only at present time. Sanland Technology Corp. reserves the right to make any changes to the specifications in this datasheet without prior notice.



Caution: ESD Sensitive

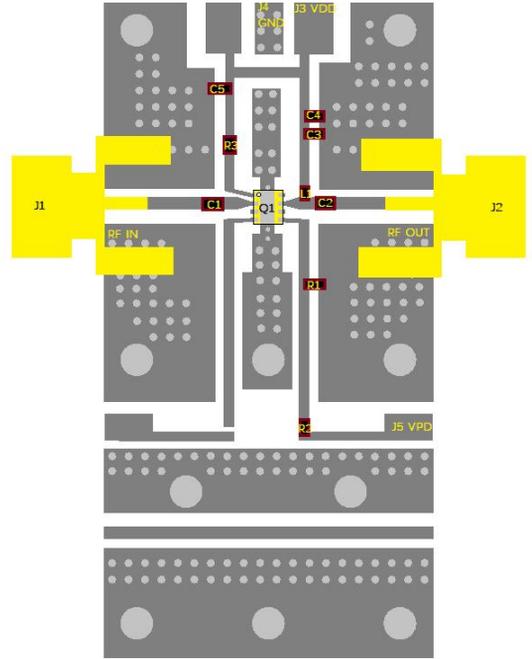
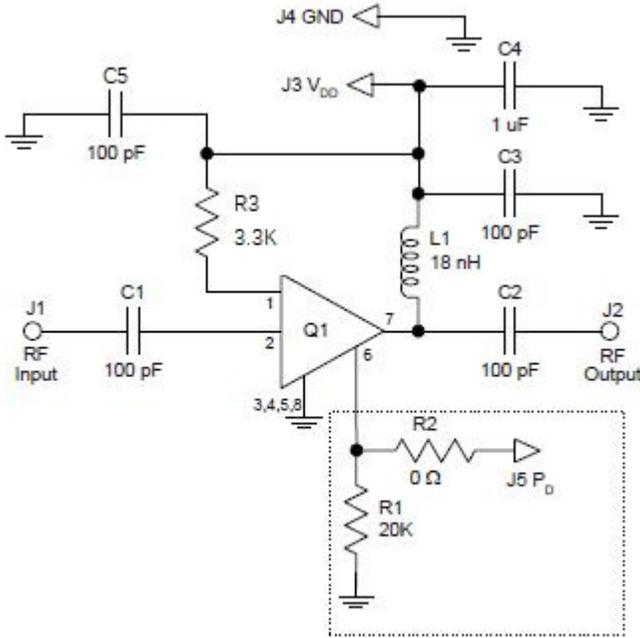
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2021.12

700 to 4200 MHz Optimized Tuning

Parameter	Specification			Units	Notes
	Min	Typ.	Max		
RF Specifications					
NF		0.6		dB	2.6 GHz, includes Evaluation Board loss
S21		24.3		dB	2.6 GHz
S11		8.7		dB	2.6 GHz
S22		19.8		dB	2.6 GHz
S12		35.9		dB	2.6 GHz
OIP3		33.7		dBm	2.6 GHz, $\Delta f = 1$ MHz, PIN = -25 dBm/tone
OP1dB		18.1		dBm	2.6 GHz
DC Specifications					
VDD		5		V	
IDQ		55		mA	Set with external resistor
Test Conditions: VDD = 5 V, TA = +25 °C, PIN = -25 dBm, Characteristic Impedance [ZO] = 50 Ω , Unless Otherwise Noted					

2021.12



Notes:

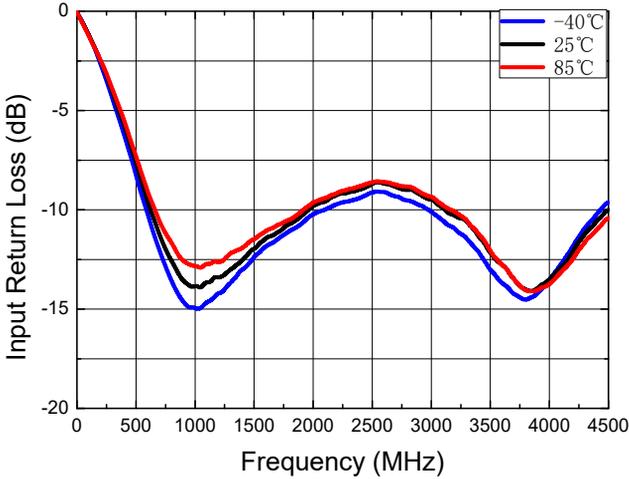
For TDD Applications: R1=20K & R2=0K.

For FDD Applications: R1=20K 'OR' Pin 5 tied to ground. R2=DNP/Omitted.

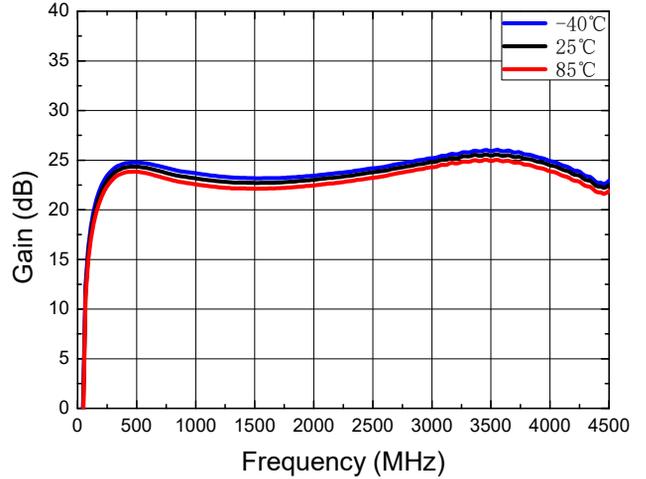
Component	Description	Value	Size	Manufacturer	Part Number
Q1	Ultra Low Noise, Flat Gain LNA			SANLAND	AL411
L1	Inductor	18nH	0402	Coilcraft	0402CS-18NXJL
C1,C2,C3,C5	Capacitor	100pF	0402	Murata	GRM1555C1H101JA01D
R3	Resistor	3.3kΩ	0402	Kamaya	RC1/4332JB
C4	Capacitor	1uF	0402	Murata	GRM31MR71H105MA88L

2021.12

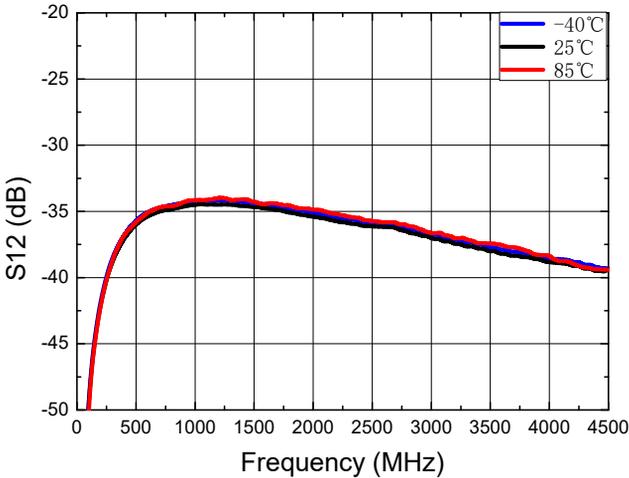
Input Return Loss Vs. Frequency



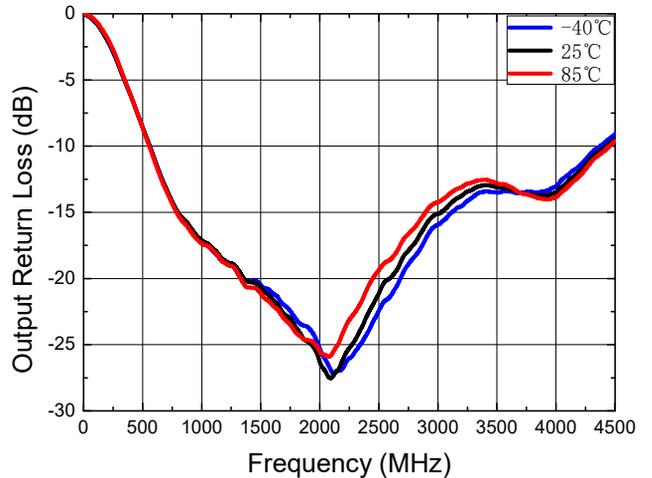
Gain Vs. Frequency



S12 Vs. Frequency

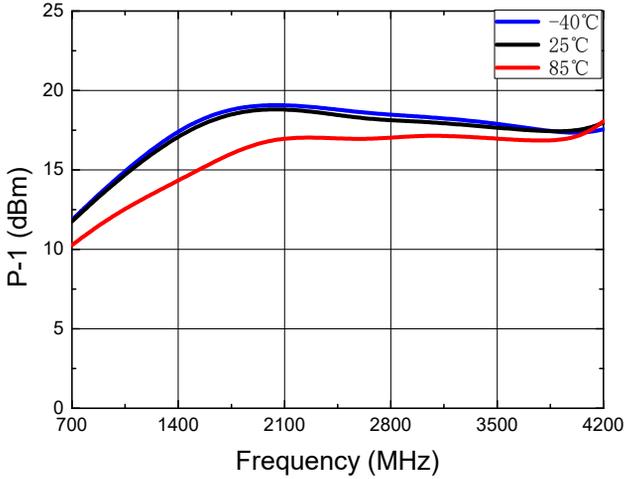


Output Return Loss Vs. Frequency

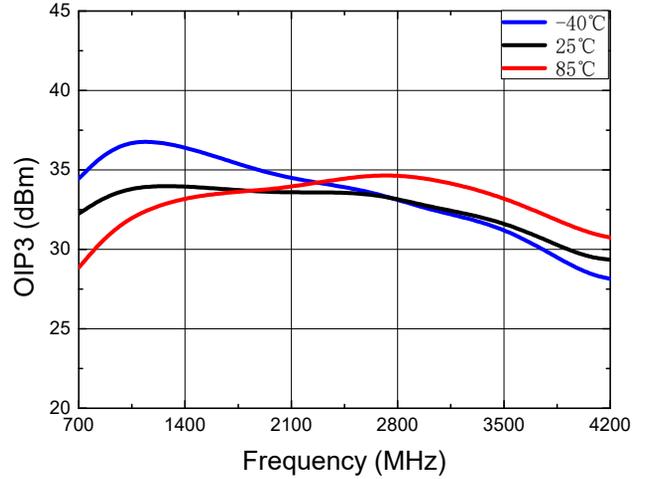


2021.12

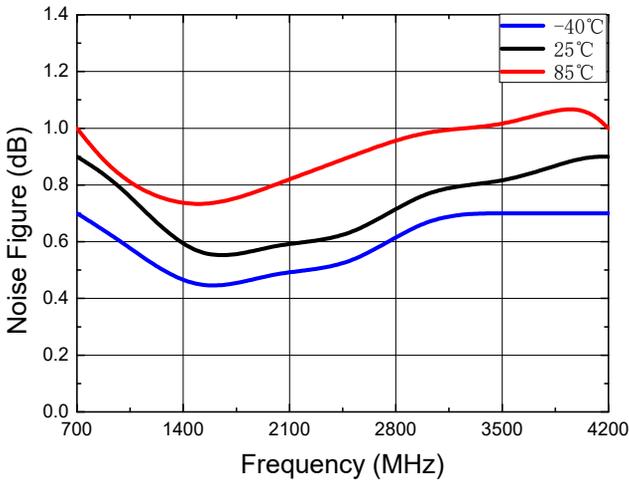
P-1 Vs. Frequency



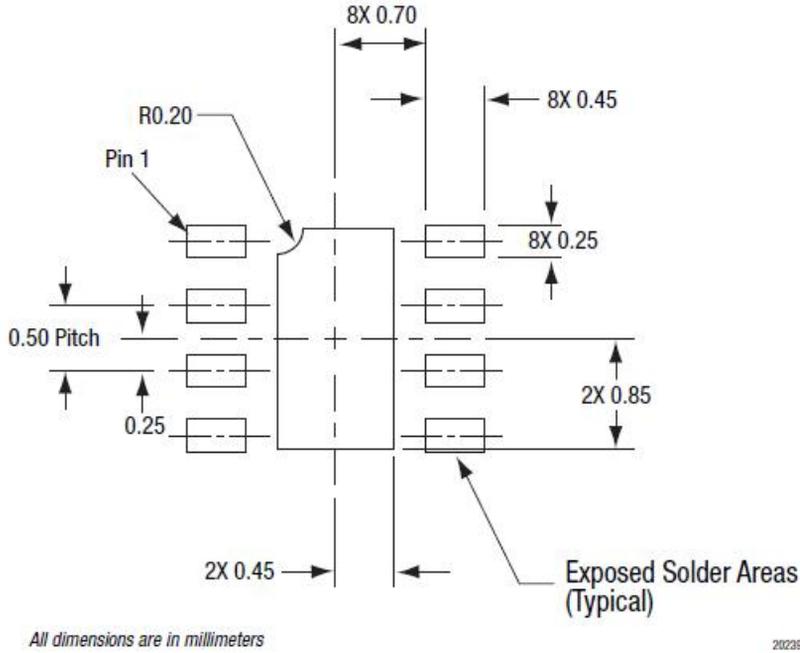
OIP3 Vs. Frequency



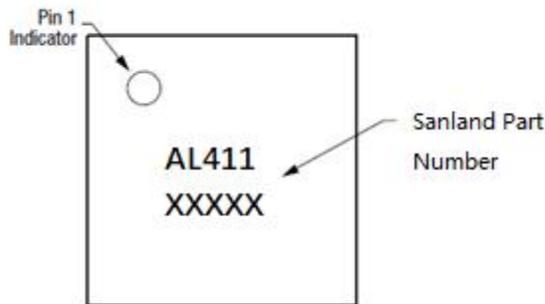
Noise Figure Vs. Frequency



2021.12

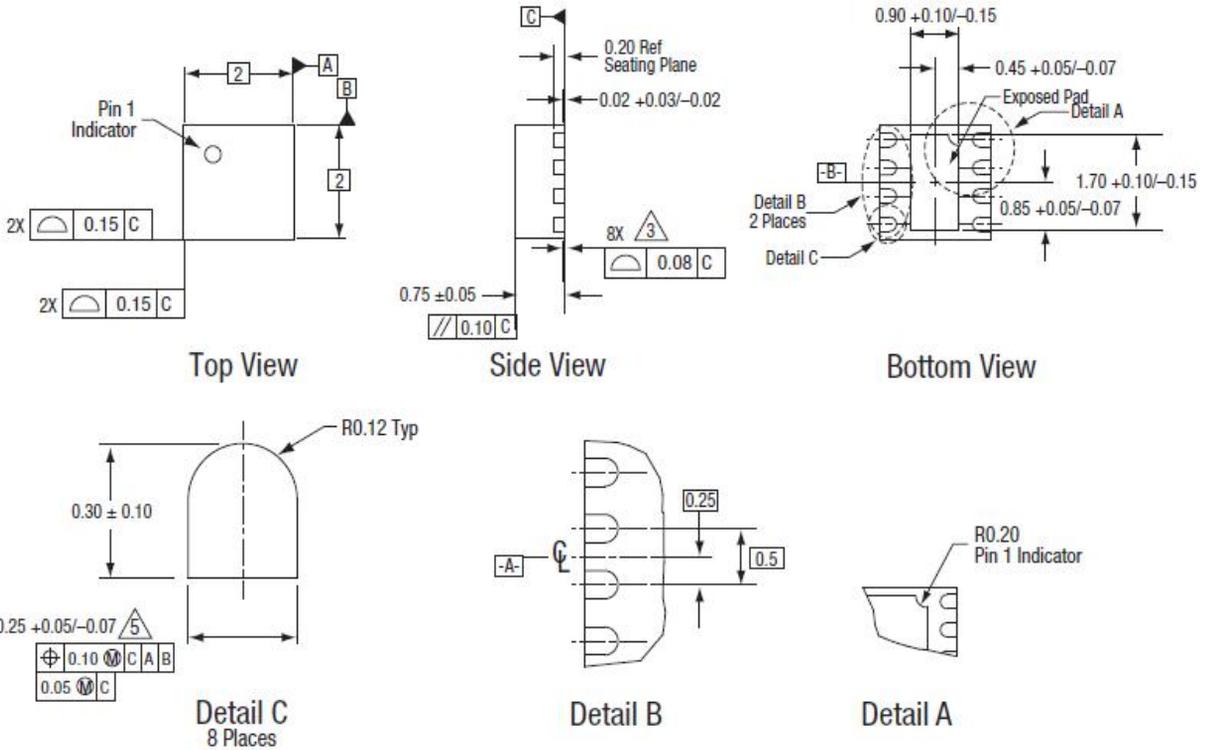


PCB Layout Footprint (Top View)



Typical Part Markings (Top View)

2021.12



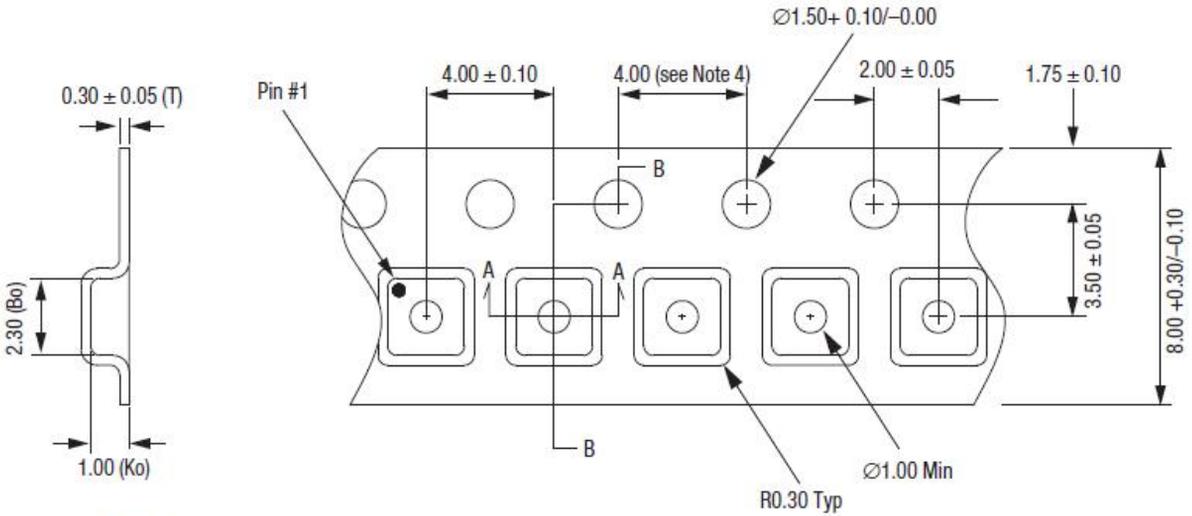
Notes:

1. All measurements are in millimeters.
2. Dimensions and tolerances according to ASME Y14.5M-1994.
3. Coplanarity applies to the exposed heat sink ground pad as well as the terminals.
4. Plating requirement per source control drawing (SCD) 2504.
5. Dimension applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

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Package Dimensions

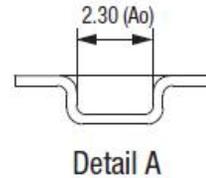
2021.12



Detail B

Notes:

1. Carrier tape: black conductive polystyrene.
2. Cover tape material: transparent conductive HSA.
3. Cover tape size: 5.40 mm width.
4. Ten sprocket hole pitch cumulative tolerance = ± 0.20 mm.
5. ESD surface resistivity is $\leq 1 \times 10^8$ Ohms/square per EIA, JEDEC tape and reel specification.
6. Ao and Bo measurement point to be 0.30 mm from bottom pocket.
7. All measurements are in millimeters.



Detail A

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Tape and Reel Dimensions